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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,730	12/09/2003	Maneesh Soni	3226.1024-001	5151
21005	7590	03/08/2007	EXAMINER	
HAMILTON, BROOK, SMITH & REYNOLDS, P.C.			FLORES, LEON	
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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE		DELIVERY MODE	
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/731,730	SONI ET AL.	
	Examiner	Art Unit	
	Leon Flores	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 09 December 2003.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-14 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) Claim(s) _____ is/are allowed.
6) Claim(s) 1-14 is/are rejected.
7) Claim(s) _____ is/are objected to.
8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 09 December 2003 is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
4) Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) Notice of Informal Patent Application
6) Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claims (3-7 & 11-12) are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

3. Re claims 3 & 7, When a claim makes reference to an industry standard, such as “802.11”, it may be rejected under 112/2d as being indefinite, as rules change over time. Therefore, it is inappropriate to have the scope of a claim change with time. Since the organizations implementing standards meet regularly and have the authority to modify standards, any connection a claim may have to these standards may have varying scope over time. The other aspect arising from this is enablement. If the regulation or standard changes, the disclosure may no longer support the limitation. An argument posed by applicant might be, “the standard being applied is that which is in effect as the day of filing of the application.” If the original specification supports this, i.e. provides a dated regulation or standard, then most likely this is not an 112/2d rejection. If it is essential material, applicant may be required to bodily incorporate this material. Likewise if the standard is so common that its meaning is definite, such as RS-235 interface, a 112/2d rejection would not be appropriate. Claims 4-7 depend on claim 3. And claim 12 depends on claim 11.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims (1 & 14) is rejected under 35 U.S.C. 102(b) as being anticipated by Miller et al (hereinafter Miller) (US Patent 4,368,434).

4. Re claim 1, Miller discloses a method of processing samples comprising: reading the samples into a tapped delay chain (See fig. 1: the input of element 20 & see col. 12, line 23); processing samples from taps on the delay chain (See fig. 3 & col. 12, line 24); subsequent to a processing event, shifting samples rapidly from the delay chain at a higher rate than samples coming in (See col. 4, lines 24-26 & 42-46); and reducing the length of the delay chain. (See col. 4, lines 22-24, col. 5, lines 52-60)

5. Claim 14 is a system claim corresponding to method claim 1. Hence, the steps performed in method claim 1 would have necessitated the elements in system claim 14. Therefore, claim 14 has been analyzed and rejected w/r to claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. **Claims (8-9 & 12-13) are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al (hereinafter Miller) (US Patent 4,368,434), as applied to claim 1 above, in view of Alexander (US Patent 6,765,419 B2).**

7. Re claim 8, Miller discloses a method of processing samples of a data packet comprising: reading the samples from a data packet into a tapped delay chain comprising a plurality of pipelined registers (See fig. 1: the input of element 20 & see col. 12, line 23); processing samples from taps on the delay chain to synchronize a data packet (See fig. 3 & col. 12, line 24); subsequent to synchronization of the data packet, shifting samples rapidly from the delay chain at a higher rate than samples coming in (See col. 4, lines 24-26 & 42-46); repeating the steps of shifting samples rapidly and reducing the length of the delay chain. (See col. 12, lines 23-27. Furthermore, samples are shifted successively.)

But the reference of Miller fails to specifically disclose reducing the length of the delay chain by bypassing empty registers.

However, Alexander does. (See col. 5, lines 26-30 & 39-44 & col. 8, lines 10-15.) Alexander discloses a delay lock loop comprised of a forward delay unit, a feedback delay unit, a comparator, a control unit, & a enable/disable logic unit. The forward delay circuit includes a plurality of individual delay elements. A predetermined number of delay elements are grouped into respective delay blocks. Forward delay circuit receives enable signal from enable/disable logic to selectively deactivate one or more of the delay blocks that are not in use.

Therefore, taking the combined teachings of Miller & Alexander as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system of Miller in the manner as claimed, as taught by Alexander, for the benefit of reducing power consumption. (See col. 8, line 15)

8. Claim 9 is a system claim corresponding to method claim 8. Hence, the steps performed in method claim 8 would have necessitated the elements in system claim 9. Therefore, claim 9 has been analyzed and rejected w/r to claim 8.

9. Re claim 12, the combination of Miller and Alexander further disclose a timing recovery module for synchronization of the data packet that initiates a transition in the processor. (In Alexander, see col. 2, lines 18-22)

10. Claim 13 is a system claim corresponding to method claim 8. Hence, the steps performed in method claim 8 would have necessitated the elements in system claim 13. Therefore, claim 13 has been analyzed and rejected w/r to claim 8.

11. Claims (1-2 & 10) are rejected under 35 U.S.C. 103(a) as being unpatentable over Alexander (US Patent 6,765,419 B2) in view of Davies et al (hereinafter Davies) (EP 0980186 A2).

12. Re claim 1, Alexander discloses a method of processing samples comprising: reading the samples into a tapped delay chain (See fig. 2: the input at element 52); processing samples from taps on the delay chain (See fig. 2: the signals are entered in the the delay chain for processing); subsequent to a processing event, shifting samples rapidly from the delay chain (See fig. 3 & col. 6, line 42-43. Furthermore, the signals entering the delay chain may be processed and shifted by the delay elements.); and reducing the length of the delay chain. (See col. 6, lines 16-22).

But the reference of Alexander fails to specifically disclose that shifting samples rapidly from the delay chain at a higher rate than samples coming in. However, Davies does. (See paragraphs 22-23.) Davies discloses a method for preventing overflows and underflows in a decoder buffer. Underflow occurs when the frame rate into the buffer is lower than the rate at which frame data is being removed. Overflow occurs when the frame rate in the buffer is greater than the rate at which frame data is removed from the buffer.

Therefore, taking the combined teachings of Alexander & Davies as a whole. It would have been obvious to one of ordinary skill in the art to have modified the rate at which frame data is entering and leaving the buffer in the system of Alexander, as taught by Davies, for the benefit of allowing the buffer to empty. (See paragraph 11)

13. Re claim 2, the combination of Alexander and Davies further discloses that wherein the samples are from a data packet. (In Davies, see abstract. Furthermore, in digital video broadcasting, large amounts of data are encoded and transmitted, as packets, to decoders having a decoder buffer.)

14. Claim 10 is a system claim corresponding to method claim 2. Hence, the steps performed in method claim 2 would have necessitated the elements in system claim 10. Therefore, claim 10 has been analyzed and rejected w/r to claim 2 above.

15. **Claims (3-7 & 11) are rejected under 35 U.S.C. 103(a) as being unpatentable over Alexander (US Patent 6,765,419 B2) & Davies et al (hereinafter Davies) (EP 0980186 A2), and further in view of applicant's prior art.**

16. Re claim 3, the combination of Alexander & Davies fails to specifically disclose that wherein the data packet conforms to 802.11 standards.

However, applicant's prior art does. (See paragraphs 2-4) Applicant's prior art discloses that, under 802.11a, packets are mapped into a framing format suitable for sending and receiving user data and management information between two or more stations.

Therefore, taking the combined teachings of Alexander, Davies, & Applicant's prior art as a whole. It would have been obvious to one of ordinary skill in the art to have incorporated the 802.11 standards in the system of Alexander, as modified by Davies and as taught by applicant's prior art, for the benefit of locating the field boundaries. (See paragraph 3)

17. Re claim 4, the combination of Alexander, Davies & Applicant's prior art further disclose that wherein the event includes a synchronization of the data packet. (In Alexander, see col. 4, lines 7-15)

18. Re claim 5, the combination of Alexander, Davies & Applicant's prior art further disclose that wherein the delay chain comprises a plurality of pipelined registers. (In applicant's prior art, see paragraph 4.)

19. Re claim 6, the combination of Alexander, Davies & Applicant's prior art further disclose that wherein the method is repeated to further reduce the length of the delay chain. (In Alexander, see col. 2, lines 15-22, col. 6, lines 4-22. Furthermore, the length of the delay line is adjusted until the incoming signal is time-aligned with the feedback

signal.)

20. Re claim 7, the combination of Alexander, Davies & Applicant's prior art further disclose that wherein reducing the length of the delay chain is performed by bypassing empty registers. (In Alexander, see col. 5, lines 26-30 & 39-44 & col. 8, lines 10-15.)

21. Claim 11 is a system claim corresponding to method claim 3. Hence, the steps performed in method claim 3 would have necessitated the elements in system claim 11. Therefore, claim 11 has been analyzed and rejected w/r to claim 3 above.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon Flores whose telephone number is 571-270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LF
February 21, 2007

David C. Payne
DAVID C. PAYNE
PRIMARY PATENT EXAMINER